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Design of Low Power Data Preserving Flip Flop Using MTCMOS Technique

Guguloth Sreekanth, Neelapala Sai Sruthi, Ravindar Nunavath

Department Of Electronics and Communication Engineering, Holy Mary Institute of Technology and Science Hyderabad, India

Abstract— *In order to reduce overall power consumption, a well-known technique is to scale supply voltages. However, to maintain performance, device threshold voltages must scale as well, which will cause sub threshold leakage currents to increase exponentially. The sub threshold voltage has to affect the two parameters one is the delay and other one is the sub threshold leakage current. Smaller the threshold voltage smaller will be delay while larger will be the sub threshold current. Controlling sub threshold leakage has been explored significantly in the literature, especially in the context of reducing leakage currents in burst mode type circuits, where the system spends the majority of the time in an idle standby, or sleep, state where no computation is taking place. MTCMOS or multi-threshold CMOS has been proposed as a very effective technique for reducing leakage currents during the standby by state by utilizing high sleep devices to gate the power supplies of a low logic block. Although MTCMOS circuit techniques are effective for controlling leakage currents in combinational logic, a drawback is that it can cause internal nodes to float, and cannot be directly used in standard memory cells without corrupting stored data. As a result, several researchers have explored possible MTCMOS latch designs that can reduce leakage currents yet maintain state during the standby modes.*

In this work a data preserving flip flop with reduced leakage power is designed using MTCMOS technique in 90nm technology with the help of CADENCE tool. The simulation results have shown that the leakage power is reduced by 25.70% compared to CMOS flip flop.

Keywords--Combinational crcuit, flipflop, Leakage power, MTCMOS technique, Sub threshold leakage current.

I. INTRODUCTION

Low power circuit operation is becoming an increasingly important metric for future integrated circuits. As portable battery powered devices such as cell phones, pagers and portable computers become more complex and prevalent; the demand for increased battery life will require designers to seek out new technologies and circuit techniques to maintain high performance and long operational lifetimes.

In modern digital CMOS integrated circuits, power consumption can be attributed to three different components: short circuit, leakage, and dynamic switching power. In modern high performance integrated circuits, more than 40% of the total active mode energy can be dissipated due to the leakage currents. As we are going from one technology generation to the next technology generation, the leakage power component is increasing and in 70 nanometer technology, the leakage power dissipation has overtaken the dynamic power. With more transistors integrated on die, leakage currents will soon dominate the total energy consumption of high performance ICs. The sub threshold leakage current is one of the most dominant leakage current components. It is the drain to source leakage current when the transistor is off, i.e., the applied voltage is less than the threshold voltage.

II. MOTIVATION

High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. So in this presentation we are tried to reduce the leakage power which is the one of the major component in the power considerations.by referring the so many papers from IEEE and from various text books .We use the technique called MTCMOS technique which reduces leakage power in CMOS gate. We applied the same technique to Flip Flop.

III. LEAKAGE POWER CONSUMPTION

The leakage power consumption, consists of two kinds of leakage currents i) the reverse-bias diode leakage at the transistor drains and ii) the sub-threshold current through an turned-off transistor channel. However, these components are technologically-controlled and thus, the designer has a few things to do about their minimization .Diode leakage occurs when a transistor is turned-off, the other ON transistor charges up/down the drain with the respect to the forme's substrate potential. The PMOS transistor with negative bias of gate with respect to substrate. So, the diode

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composed by drain diffusion and substrate is reversely-biased.

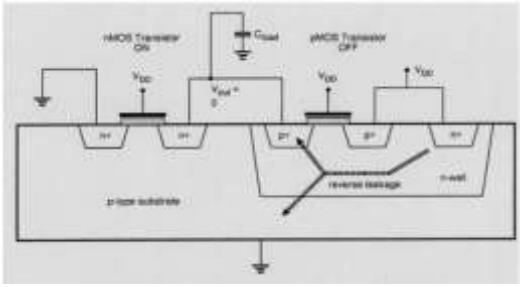

Fig 1: Reverse leakage current path in CMOS inverter

3.1 MTCMOS TECHNIQUE

Multi-threshold CMOS (MTCMOS), which is also known as power/ground gating, is the most commonly used leakage power suppression technique in state-of-the-art integrated circuits. Significant power and ground distribution network noise is produced when an MTCMOS circuit blocks transitions from SLEEP mode to ACTIVE mode. The reliability of the surrounding active circuit blocks is seriously degraded. Power and ground distribution network noise that is produced during mode transitions is the most important reliability concern in MTCMOS circuits. A variety of mode transition noise mitigation techniques that are applicable to MTCMOS circuits are investigated in this dissertation. Novel MTCMOS memory circuits with enhanced speed and suppressed leakage power consumption are proposed in this dissertation.

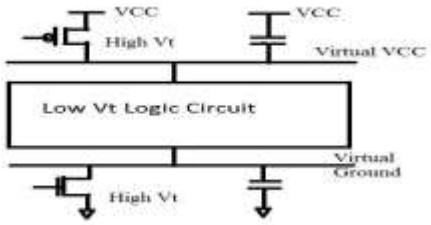

Fig 2: MTCMOS circuit structure showing both polarity sleep devices.

3.2 Data loss in memory elements

The MTCMOS idea is straightforward for combinational logic but there are difficulties with sequential circuits. If the power supply is simply gated during sleep mode, the state of the circuit is loss and cannot be recovered when returning to active mode . The retrieval of the previously stored data for restoring a system to a pre sleep state costs significant energy and timing overheads when the MTCMOS sequential circuits are activated .The sudden surge current also exists in floating node and might violate the reliability of the circuit. One of the problems with sequential circuits that utilize feedback and parallel devices is that sneak leakage paths may exist. Sneak leakage path can arise in MTCMOS circuits whenever the output of an MTCMOS gate is electrically connected to the output of a CMOS gate. In fact, the interfacing between MTCMOS type circuits and CMOS type circuits is what gives rise to potential leakage paths.

IV. MTCMOS BASED FLIP FLOP

A number of methodologies have been reported in the literature to solve the issues that affect the performance of the MTCMOS circuit. Several MTCMOS techniques based on charge recycling between the virtual rails and the sleep signal lines are presented in for suppressing the energy overhead of mode transitions. These techniques require complicated timing control circuitry to enable charge recycling during the mode transitions. These techniques also significantly increase the system wake-up delay, thereby degrading the system performance. In both gated and gated ground techniques are employed in a charge recycling MTCMOS circuit. A pass transistor is placed between the virtual power and virtual ground to allow charge recycling. Another proposed technique is employed a pass transistor for charge recycling between virtual rails and sleep signal lines. The sleep transistor is driven by a tri-state buffer and a high- pass transistor is allowed charge recycling between virtual rail and sleep signal. Sequential MTCMOS circuits require more care since they must hold state in standby mode. The previously published MTCMOS flip flop.

4.1 5Transistor D- Flip Flop using MTCMOS

A Flip Flop is a circuit that has two stable states and can be used to store state information. Different type of Flip Flops signifies the way in which binary information enters a flip-flop, binary state maintained by a flipflop circuit indefinitely(as long as power power is delivered to the circuit) until directed by an input signal to switch states.TSPC stands for True Single Phased Clocked logic in which we only have one clock and do not need an inverted clock.there are several benefits with this technique such as the elimination of skew due to different clock phases and clock signal being separated off chip,which implies significant savings in chip area and power consumption.The below figure is showing the 5T TSPC D flipflop with MTCMOS technique.Two transistors P3 and N4 are used in the circuit.The transistor N4 is supplied with signal SL (sleep) and transistor P3 is supplied with signal SL"(complement of sleep) SL and SL" transistors are

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supplied with high threshold voltages. When SL signal is low SL‟ is high, there will be no current flow in low threshold voltage main circuit. When SL is high and SL‟ is low circuit works in normal mode.

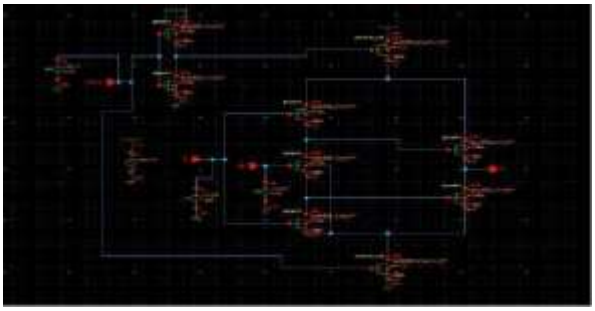

Fig.3: Schematic Diagram of 5T Flip Flop

The output waveform of the flip flop is shown below:

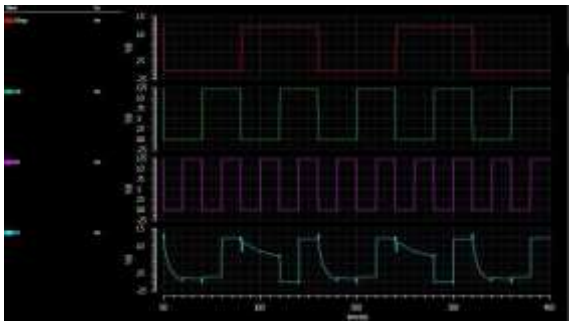

Fig 4: Transient analysis of MTCMOS based 5T Flip Flop

4.2 Problem with 5T Flip Flop

The 5 transistor D-flip flop designed using MTCMOS technique has problem during the sleep mode. The 5 transistor is working normal in the active mode while in the sleep mode the flip flop is not able to retain the data during the standby mode as the low circuit is floating during sleep mode. Therefore the flip flop circuit needs to be modified so that it can preserve data during sleep mode and there should be low leakage path in the circuit.

V. PROPOSED MTCMOS BAESD FLIP FLOP

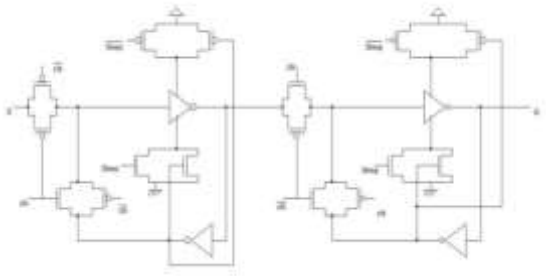

Fig 5: Proposed MTCMOS based Flip Flop

5.1 Operation of the Circuit

The proposed flip-flop utilizes parallel high Vt devices in both the master and slave stages. Both flip flops recirculate data in the master stage and provide CMOS compatible outputs, but the leakage feedback flip flop has better performance characteristics. During the active mode, the leakage feedback flip flop behaves exactly like a standard master slave flip flop, as the helper high Vt devices are only used to retain state during the standby state. When either the master or slave latch is in the holding state, the feedback path is turned on, and the stored value is recycled through cross coupled inverters. During the standby condition, data is stored in the master latch, with the clock held high .The leakage feedback gate switches the appropriate helper high device on such that the previously held data in the master stage is actively maintained.

VI. SIMULATIONS AND RESULTS

Cadence Design Systems is an American electronic design automation (EDA) software and engineering services company, founded in 1988 by the merger of SDA Systems and ECAD, Inc. The company produces software for designing integrated circuits (also known as "chips"), and printed circuit boards. Cadence tools is used to do simulations. Here we used NMOS 1v and PMOS 1v transistors are used to design the circuits.

6.1 D Flip Flop Schematic diagram

The schematic diagram of D-Flip Flop is shown in the fig 6 and transient analysis of this circuit is shown in fig 7. The sizing of the transistor is necessary to work properly of the Sleep transistor. Transient analysis has been done for 50 ns time interval. The input pulse width 2ns and period 4ns with amplitude 1.8V and 1.2V for doing the transient analysis. The pulse width of clock used is 8ns.

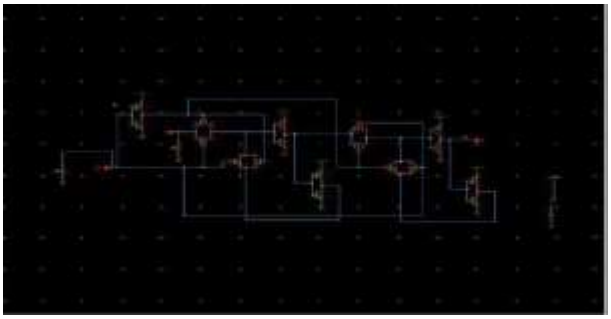

Fig.6: Schematic Diagram of D-Flip Flop

The transient analysis of the circuit is done and the output waveform is shown below. The analysis has been done for 50ns. The output is obtained at the frequency 250 MHz at a supply of 1.2V.

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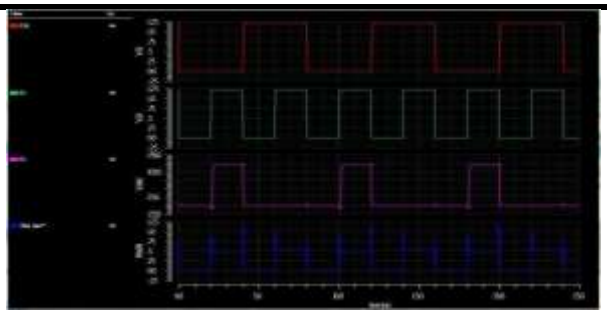

Fig 7: Transient analysis of D-Flip Flop

VII. PROPOSED MTCMOS BASED FLIP FLOP SCHEMATIC DIAGRAM

The schematic diagram of proposed MTCMOS based D-flip flop is shown in the figure 5.4 and transient analysis of this circuit is shown in fig 5.5. The sizing of the sleep transistor is necessary to work properly of the pulse generator. Transient analysis has been done for 50 ns time interval. The input pulse width 4ns and period 4ns with amplitude 1.8V for doing the transient analysis. The input pulse width for the sleep signal is taken as 8ns with period of 16ns.

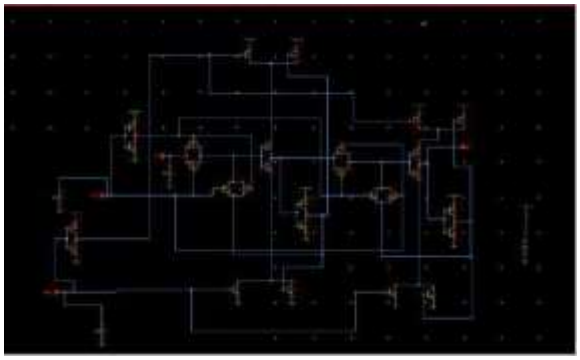

Fig.8: Schematic of MTCMOS based Flip Flop

The transient analysis of the MTCMOS based flip flop is done and the output waveform is shown below at a frequency of 250 MHz

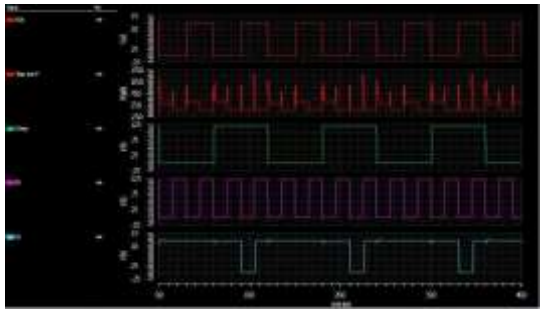

Fig.9: Transient Response of MTCMOS based Flip Flop

VIII. RESULT

The transient power and delay of the both the circuit is calculated at two different supply voltages. The comparison of power and delay is shown in the Table 1.

Table 1: Power and Delay comparison of Flip Flop Design

Data clock	FlipFlop	MTCMOS based flip flop	Power Saving (%)	Avg Power Saving (%)
0 0	188.28 E-9	112.40 E-9	40.30	25.70
0 1	215.32 E-9	173.30 E-9	19.52	
1 0	164.2 E-9	122.80 E-9	25.21	
1 1	200.98 E-9	165.20 E-9	17.80	

The leakage power comparisons in standby mode of various flip-flop is summarized in table II. We applied four test patterns(0,0), (0,1) ,(1,0) and (1,1) by changing clock and data.The leakage power is calculated while keeping the sleep transistors in off state. Since the sleep transistor is off the low Vth circuit is floating as a result the leakage power is minimized. The comparison of leakage power of both the circuit is shown in the Table 2.

Table.2: Leakage Power Comparison in standby mode (nw)

Data clock	FlipFlop	MTCMOS based flip flop	Power Saving (%)	Average Power Saving (%)
0 0	188.28 E-9	112.40 E-9	40.30	25.70
0 1	215.32 E-9	173.30 E-9	19.52	
1 0	164.2 E-9	122.80 E-9	25.21	
1 1	200.98 E-9	165.20 E-9	17.80	

IX. CONCLUSION

With the continuous scaling of CMOS devices, leakage current is becoming a major contributor to the total power

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consumption. In current deep sub-micrometer devices with low threshold voltages, sub-threshold and gate leakage have become dominant sources of leakage. Power gating techniques have become very common in literature and in practice, and MTCMOS implementations in particular have demonstrated significant improvements in standby power consumption. The overall leakage power consumption of proposed flip flop has reduced by 25.70% on average. There is also improvement in overall power consumption as well as in speed of operation.

FUTURE SCOPE

When a conventional sequential MTCMOS circuit transitions from the sleep mode to the active mode, significant bouncing noise is produced on the power and ground distribution networks. The reliability of the surrounding active circuitry is seriously degraded. Therefore the work can be done in reducing the noise in the circuit so that the circuit performance enhances more.

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